Catastrophic Latchup in CMOS Analog-to-Digital Converters

T. F. Miyahira, A. H. Johnston, H. N. Becker, S. D. LaLumondiere and S. C. Moss

***Abstract* - Heavy-ion latchup is investigated for analog-to-digital converters. Differences in cross section for various ions show that charge is collected at depths beyond 50 µm, causing the cross section to be underestimated unless long-range ions are used. Current distributions, thermal imaging and diagnostic tests with a pulsed laser were used to identify latchup-sensitive regions. Latchup in one of the circuit types was catastrophic, even when the power was turned off within 2 ms of a latchup event. Examination of damaged devices with a scanning electron microscope showed that the failures occurred in metallization and contact regions. Current density for failure agrees with pulsed current metallization stress data in the literature.**

I. INTRODUCTION

Many CMOS circuits are sensitive to latchup from heavy ions, and latchup is one of the major considerations when CMOS devices are evaluated for space applications. Radiation-induced latchup has been studied for many years [1-8], but it remains a difficult problem in actual circuits because latchup sensitivity inherently depends on the layout and distribution of contacts, power and ground within complex circuits [9].

Commercial CMOS devices are designed to withstand electrically induced latchup from transients or start-up conditions at the input, output and power supply connections, but generally do not consider triggering from *internal* transients such as those caused by heavy ions. Many CMOS devices are fabricated on so-called epitaxial substrates where a relatively thin lightly doped epitaxial region is grown over a highly doped, low resistivity substrate. Although epitaxial substrates do not necessarily eliminate latchup from heavy ions or protons in space, the increasing trend towards epitaxial construction has generally improved latchup performance in space environments.

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High-performance analog-to-digital converters are an exception. They are usually designed with bulk substrates because epitaxial substrates induce approximately three times more noise from the digital to the analog region [10]. Thus, latchup is expected to remain a critical issue for A-D converters. This paper discusses latchup in two types of CMOS analog-to-digital converters from one manufacturer. Both converters are fabricated on bulk substrates, and are sensitive to latchup from heavy ions. Most latchup events caused catastrophic failure in one device type, but not in the other. Catastrophic failure is a difficult problem to address, and has not been investigated in detail in earlier studies of latchup from heavy ions. The main purpose of this paper is to investigate the underlying reasons for such failure, along with ways to relate catastrophic failure to basic device properties.

II. EXPERIMENTAL APPROACH FOR HEAVY ION TESTING

A. Device Description and Experimental Setup

The two devices used in this study were manufactured by Analog Devices using advanced CMOS processes with a feature size of 0.6 µm. They were selected because of potential use in NASA space systems, which require high-performance converters with low power dissipation.

The first device, the AD9240, is a successive-approximation 14-bit analog-to-digital converter that incorporates three different power supplies (all 5 V). The maximum conversion rate is 10 Mb/s. One supply is used for the analog section of the part, and has the highest power consumption during normal operation (nominally 60 mA). A second power supply is used for digital circuitry in the *interior* regions of the digital part of the chip, and it typically requires about 7 mA during normal operation. A third power supply is used to provide power to the output drivers. The nominal current is only a few mA, depending on duty cycle and output loading.

The second device, the AD9260, is a 16-bit sigma-delta oversampling converter with a pipeline technology that provides high conversion rates [11]. The AD9260 also uses three 5-V power supplies, just as for the AD9240. When operating at the maximum conversion rate (20 megasamples/s), the total power consumption is 550 mW. Most of the power is consumed in the analog portion of the chip.

Both converters are only available in plastic packages. A special acid etching system was used to remove the plastic at the top surface, thereby allowing direct access to the top of the die for heavy-ion testing. For radiation tests, the devices were mounted in evaluation boards, provided as a standard item by the manufacturer for evaluation purposes. The evaluation boards are designed to minimize electrical noise and interference between the digital and analog sections of the device, and provide a far less costly alternative compared to the development of custom test fixtures.

B. *Radiation Test Approach*

Radiation testing was done by irradiating the device in the test board, monitoring functional operation and the currents in each power supply. A Hewlett-Packard 6629A power supply was used that could shut down power within about 100 ms after a high-current condition was found in any of the power supplies (a different power control system was used for laser testing that enabled power shutdown within 2 ms, which is described in Section IV-A). The current trigger conditions and current limit could be programmed separately. Rapid shutdown prevented destructive burnout for the AD9240 and minimized heating during the time that latchup occurred. However, the shutdown procedure was not effective for the AD9260; during heavy ion tests catastrophic failure occurred approximately 30% of the time except for tests at relatively low LET values.

Radiation tests were done at two different accelerators. Initial tests were done at Brookhaven National Laboratory, that provides ions with more limited range (typically 30 to 45 µm, depending on the ion type). Some tests were done at Texas A&M, where ions are available with ranges well above 100 µm. Tests at both facilities were done in vacuum, using the tuned energies of the various ion species (no beam degraders were used). Beam calibration was done by each facility, based on scintillators to count the number of particles.

Additional tests were done with californium-252 because of the low cost and convenience, and ease of studying specific latchup paths with auxiliary laboratory equipment.

III. Test and Characterization Results

A. *Heavy Ion Test Results - AD9240*

The cross section for latchup of the AD9240 is shown in Figure 1 as a function of LET. Data were obtained from several different experiments, some of which were done at an angle to increase the effective LET. The effective range (taking the incident angle into account) is shown for each data point. Counting statistics were nominally 5-8%. The ions used for this series of experiments are listed in Table 1.

Table 1. Ions Used for AD9240 Latchup Tests

Ion	Energy (MeV)	Angle	Effective LET (MeV-cm^2/mg)	Range (µm)
Cl	210	45	16.2	44
		60	23.0	31
Ni	260	0	26.6	40
		45	37.6	28
		55	46.4	23
Xe	1961	0	43.8	160

Note that the cross section is substantially higher for ions with longer range; in particular the cross section for the last data point with 23 µm range is about a factor of three lower than that of the next-to-last data point that was taken with a 160 µm range ion. Although it was not possible to measure device temperature because of the physical constraints of the evaluation boards, the mean time between successive latchup events was 10 seconds or more, so that the effect of the additional heating from the higher current condition during latchup is very small (the analog part of the circuit typically draws about 60 mA). The threshold LET was above 15 MeV-cm^2/mg. The effect of this difference in range on device behavior is consistent with charge collection in bulk substrate devices (see Dodd, et al.[12]).

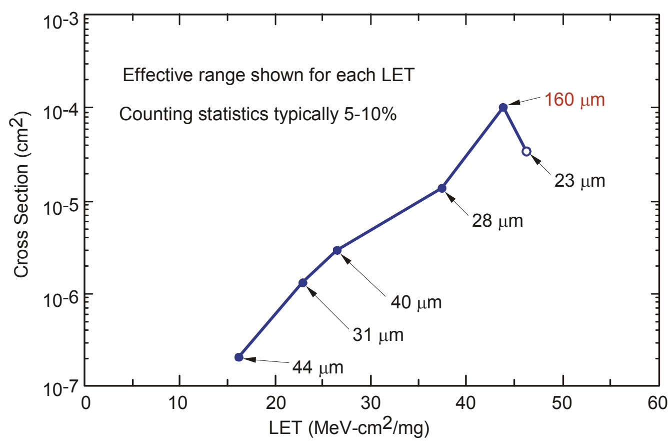


Figure 1. Latchup cross section of the Analog Devices AD9240 obtained after several different radiation tests. Note the different ranges for various points on this curve.

The cross section increases somewhat gradually over a wide range of LET values. All of the tests with heavy ions were done using somewhat conservative current limit values for the three power supplies to avoid destroying the device, and to allow a series of tests to be done on a small number of devices. The current limit values were 30 mA for the two digital power supplies (with nominal operating values of 2 to 7 mA) and 100 mA for the analog power supply (with nominal operating current 60 mA). The equilibrium current condition approximately 10 ms after latchup occurred was monitored for each latchup event. Although many of the events corresponded to full current limit for the analog power supply (100 mA), about 25% of the events resulted in an equilibrium current below that limit. Catastrophic latchup did not occur.

Tests were also done using californium ions with the current limit of all three power supplies extended to 2 A. Those tests provided better information about the equilibrium currents in typical applications where there are relatively large capacitors that can provide much higher currents compared to the restricted current from the laboratory power supply system used for the heavy ion tests. The tests done with broader current limit control showed a very wide range of latchup equilibrium currents for the digital power supply, ranging from about 45 to more than 300 mA. A histogram of the currents obtained during the tests with californium is shown in Figure 2. Similar variability occurred for currents in the analog power supply for latchup events that caused current to increase in the analog circuitry. Note that nearly all of the latchup currents were well below 200 mA.

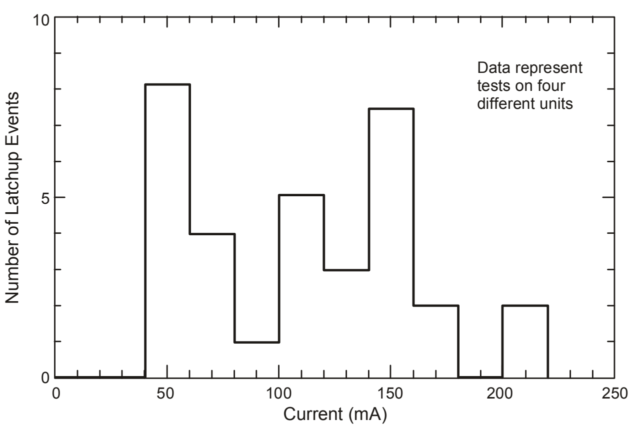
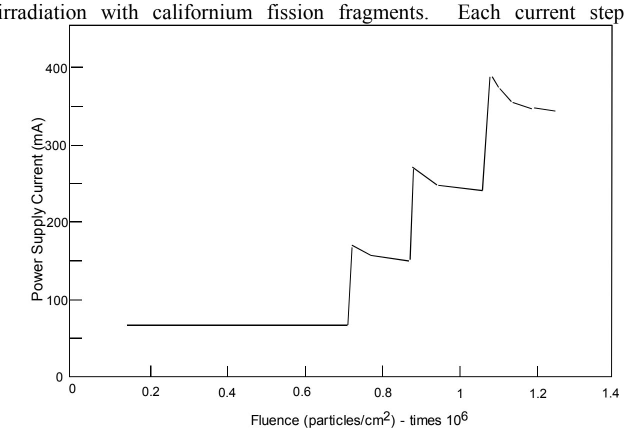


Figure 2. Histogram of many different latchup events showing the wide range of equilibrium currents in the digital power supply when the devices were irradiated (and latched) with californium. Power supply current limiting (2 A) was well above the highest latchup current

Latchup events with californium were of two types, as determined by monitoring the power supply currents. Latchup occurred either in the interior digital regions or the analog section, but never in the output drivers. Most of the latchups did not result in device destruction, even though the current limit was 2 A. Note however that ^{252}Cf is not necessarily capable of triggering events that correspond to LET above about 25 MeV-cm^2/mg because of the limited range of the californium fission fragments.

Some tests were done by leaving the device in a latched state, allowing subsequent latchup events to occur. Substantial heating of the device occurred after the first latchup event, allowing later latchup events to be more easily triggered because of the strong temperature dependence of latchup [13]. Figure 3 shows a representative test of this type in which four latchup events were observed in the analog region of the device. Note that the current drops slightly after each current "step," probably because the metallization resistance and well resistance increase due to localized heating. The last event resulted in destructive failure of the device.

Figure 3. Sequence of latchup events during tests with continual irradiation with californium fission fragments. Each current step



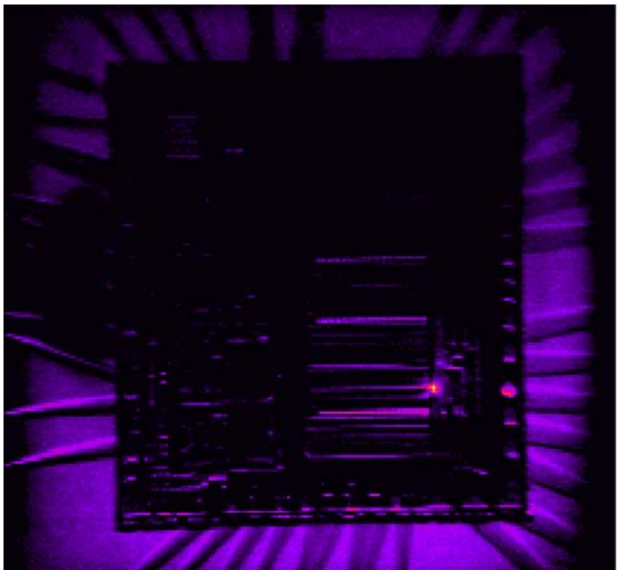
corresponds to an additional latchup event in a different region of the device.

B. *Thermal Imaging of Latched Regions*

It is very difficult to determine which internal regions of complex devices are actually involved in the latchup path. We used a thermal imaging system, coupled through an infrared microscope, to examine the surface of AD9240 devices after latchup. The imaging system contains software for automated analysis of the temperature distribution. However, the calibration is limited by the variation in thermal emissivity in different regions (areas covered by metallization have much lower emissivity than silicon regions of the chip).

Higher sensitivity (and better thermal accuracy) can be obtained by coating the device after latchup has occurred with a thin layer of black paint to provide more uniform emissivity. The paint layer was applied after latchup in order to avoid interposing material between the surface of the device and the californium ions (the thickness of the paint is difficult to control). After the initial image was taken (with the device latched and paint on the top surface), power was momentarily interrupted and the device was allowed to come to thermal equilibrium for about three minutes. At that time a second thermal image was taken. The difference between those two images was then used to measure the actual surface temperature of the device, assuming an emissivity of unity. The thermal imaging system is calibrated to read temperature in this way. Thermal measurements also provide a way to determine the approximate dimensions involved in the latchup current path, which are usually much larger than the size of the isolation well because of the extended current flow that occurs within the substrate region.

Surface temperatures of about 130 C were measured with the imaging system, as shown in Figure 4. The hot region is confined to a small region, approximately 30 μm in diameter. Temperatures below the surface are likely at a much higher temperature compared to the temperature at the surface. The region shown in the figure is within the analog region of the device.



Many regions of the AD9240 were sensitive to latchup. Figure 5 shows an outline of the die, along with regions where latchup was observed during several different irradiations with californium. After each latchup event, the device was removed from the vacuum chamber (retaining power to keep the device in a latched condition) so that the thermal imaging results correspond to equilibrium conditions with the device in air.

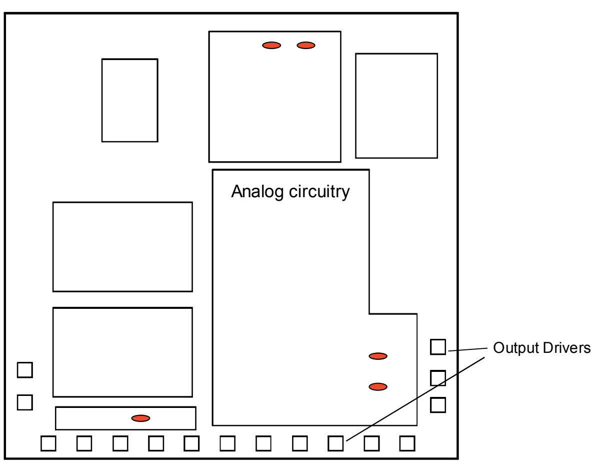


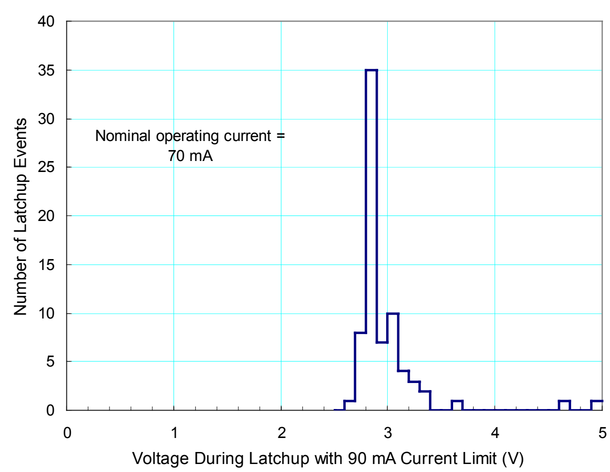
Figure 5. AD9240 latchup regions, determined by thermal imaging after tests with californium. Thermal imaging was not done during accelerator tests because of the cost for the "dead" time required to continually interrupt radiation testing to do the thermal imaging.

Snapback [14,15] can also cause circuit malfunctions when devices are irradiated with heavy ions, and snapback has many similarities to latchup. Generally the current involved in snapback is much lower because it involves only current *within* a single MOS transistor and does not involve any current flow within the substrate. The magnitude of the currents observed in our tests along with the extended thermally heated region observed with thermal imaging support the conclusion that these events are due to latchup, not snapback or a second possible mechanism, second breakdown [16].

C. Heavy Ion Results for AD9260

Although the fabrication process is essentially the same for the AD9260 as for the AD9240, most of the latchup events in the AD9260 were catastrophic. Consequently it was only possible to get latchup results with the power supply current limit set very closely to the normal power supply current and for tests with LET < 13 MeV-cm^2/mg. Most of the latchup events in the AD9260 occurred in the analog power supply. Figure 6 shows a histogram of equilibrium voltages where the current increases from a nominal 70 mA to 90 mA (the current limit setting) during latchup. The distribution of voltages provides an approximate measure of the distribution of latchup sites within the device (a similar plot for the AD9240 shows a much wider distribution of equilibrium voltages). However, the current distribution is limited to low LET values where catastrophic latchup did not occur. Current distributions were measured later using a pulsed laser, as discussed in the next section.

Figure 6. Histogram of equilibrium voltages for the AD9260 with the current limit set close to the nominal operating current.



The threshold LET for the AD9260 was 7.9 MeV-cm^2/mg, nearly a factor of two lower than that of the AD9240. The cross section was 5.1 x 10^{-7}; it increased to about 7 x 10^{-6} at an LET of 11.1 MeV-cm^2/mg. The destructive nature of the latchup events prevented us from characterizing the latchup cross section at higher LET values.

IV. Laser Testing and Identification of Catastrophic Failure Regions

A. *Experimental Approach*

The pulsed laser facility at the Aerospace Corporation was used for additional tests on the AD9260, which exhibited catastrophic failure during most of the heavy ion tests. The laser wavelength was 815 nm, corresponding to a 1/e absorption depth of 12 µm. Although the AD9260 has two levels of metallization, the structure is sufficiently open to allow the laser to penetrate most regions of the chip.

The purpose of the laser testing was to identify the regions where the AD9260 was sensitive to latchup, using a special pulsed power control system that allowed the power supply voltage to be turned off after much shorter time intervals than was possible with the heavy ion tests. The pulsed power system did not require output capacitors for stability, and could be turned on and off in time periods as short as 1 µs when driving low capacitance loads. However, the relatively large capacitors that were present on the analog development board extended the minimum time interval to about 100 µs. The power system was synchronized with the laser pulse, applying power about 10 ms before the laser pulse arrived. The time period that voltage remained on the device after the laser pulse was applied could be adjusted from 100 µs to arbitrarily longer time intervals. The power was turned off after each laser pulse, regardless of whether latchup was observed. The current through the device was observed on a digital oscilloscope during each laser pulse.

This approach reduced the time interval after latchup to much shorter time periods than was possible during tests with heavy ions. In principle this should reduce the likelihood of destroying the device. However, we still observed destructive latchup during the laser tests of the AD9260. Pulsed laser tests were also done on the AD9240 in order to compare the heavy ion test results with the laser tests. The laser tests showed that there were many different regions within the analog section that were sensitive to latchup, and generally agreed with the results from the thermal imaging experiments.

B. *Latchup Sensitive Regions in the AD9260*

A diagram of the layout of the AD9260 is shown in Figure 7, along with regions within each region that were sensitive to latchup. The digital section occupies about 30% of the chip area, and latchup could be triggered throughout that region (there are literally thousands of individual latchup sites). However, catastrophic failure was never observed when latchup occurred in the digital circuitry. Current during latchup in the digital section was typically between 40 and 60 mA.

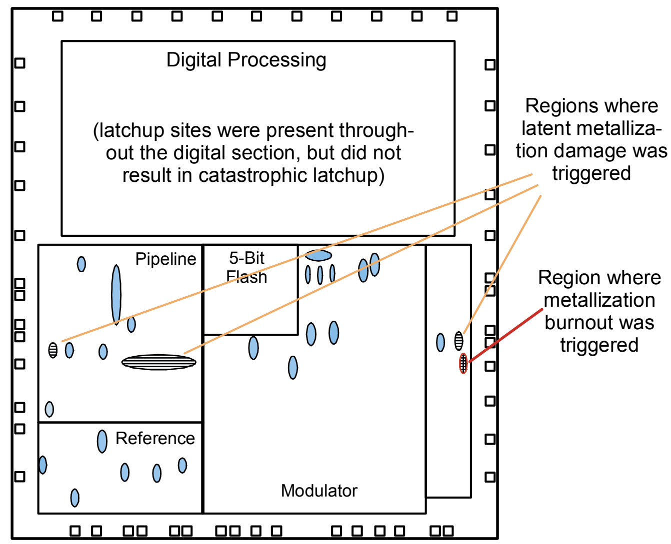


Figure 7. Diagram of the AD9260 showing latchup-sensitive regions.

Latchup also occurred in many other regions of the device where the circuitry is less regular than for the digital section. Approximately 28 latchup-sensitive sites were observed with the laser; that is, 28 general regions with distinctly different geometries and equilibrium currents. Within each general region there were numerous individual sites. The latchup current and the minimum laser power required to initiate latchup depended on the specific location of the laser spot.

C. *Catastrophic Failure*

The complexity of the AD9260 makes it extremely difficult to identify regions where catastrophic failure occurs from heavy ions because there are so many different latchup-sensitive regions, and there are very few clues about where to examine the device for failed regions. Laser irradiation overcomes these difficulties.

Several parts exhibited catastrophic failure during laser testing. All of the failures appeared to be associated with metallization or contacts that were present in the overall current path, but physically quite distant from the region where latchup actually occurred.

Another interesting observation was that irradiating different devices in the same general area produced nearly identical failures; that is, the regions where metallization or contact failure occurred were essentially the same for different devices, and was caused by the basic topology of the circuit, not by local defects in metallization.

An example of metallization failure is shown in the scanning electron microscope photograph of Figure 8. The pulsed current through this region was >200 mA for the short time period that this current flowed through the metallization region prior to failure.

(a) Appearance of failed region before the silicon nitride layer was removed.

(b) The same region after removal of silicon nitride.

Figure 8. Scanning electron microscope photograph of metallization

failure induced by latchup.

Figure 8a shows the appearance of the failed region before the layer of silicon nitride, which surrounds the top metal layer, was removed. In this case a slight crack is evident in the nitride region, along with a "droplet" of aluminum metal that extends laterally from the metal stripe. Figure 8b shows the same region after the nitride layer was removed. It is evident from the second photo that metal was ejected from the region above the metal "droplet". Although the SEM photograph in Figure 8 is for failure triggered by a laser, heavy-ion-induced failures produced the same sort of damage in the same general region of the chip.

Metallization damage did not always cause failure. There were numerous cases where aluminum had clearly been ejected from the metallization (encased in silicon nitride) but the device still functioned properly. In some of the laser tests a large increase in current was observed on a digital oscilloscope that decreased below the pre-irradiation value before the power source was shut off (recall that the power source was shut off after each pulse, regardless of the current value). This is the same signature that was observed when the latchup was catastrophic. Our interpretation of this result is that the heating, melting, and subsequent ejection of part of the encased aluminum caused the metal line to be temporarily open, but that the subsequent solidification bridged the internal gap in the conductor. Later SEM photos showed many cases where this type of mechanism was likely.

Figure 9 shows a representative example where metallization appears to "bridge" the damaged region. This implies that latent damage may be present in metallization lines even if latchup is not catastrophic.

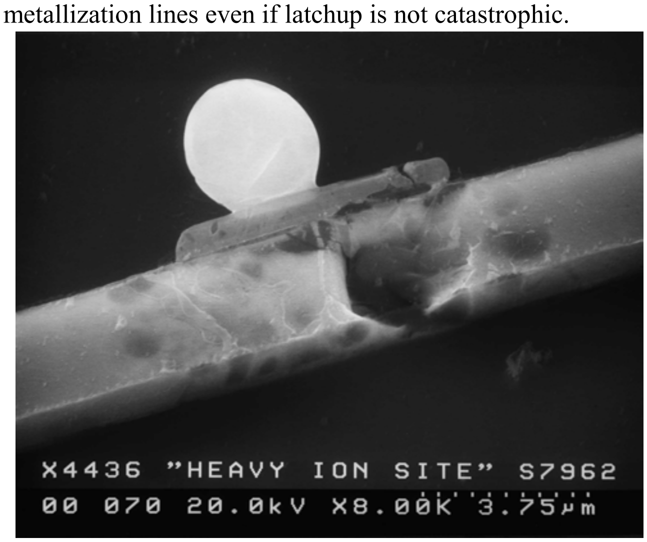


Figure 9. SEM photo of a region damaged from current during latchup where the metallization line remains conductive even though metal has been ejected from over 90% of the conducting metal line.

In addition to examining the regions where metallization failures occurred we also used the scanning electron microscope to investigate the region where the laser pulse triggered latchup; i.e. the region where high current was present in the well and substrate region during latchup. Those regions were often located well away from the metal line where the catastrophic failure occurred, as far as 60 µm. No physical changes were evident in the semiconductor regions, implying that metallization failure was the underlying cause of catastrophic failure from latchup.

V. Discussion

A. General Considerations

Latchup in these analog-to-digital converters shows the complexity of latchup in modern devices. A number of issues have to be considered.

First, for devices with bulk substrates it is essential that the effective range of the ions used for testing is above 40 µm because charge collection occurs deep within the substrate. If ions with shorter range are used the cross section will be too low. It is also possible to overestimate the threshold LET value by a considerable amount because the latchup threshold will be higher for short range ions due to the decreased charge deposition. This can introduce significant errors in estimating latchup failure rates in space applications.

Second, current limiting has to be used very cautiously when latchup tests are done. If the current limit is too low it may prevent some latchup events from occurring, underestimating the cross section and causing catastrophic latchup to be missed. For the AD9240, current limiting of the digital power supply caused the analog section to be loaded down when latchup occurred in the digital region, erroneously indicating that all latchup events occurred in the analog region of the circuit. Subsequent tests with higher current limits showed that latchup could occur in digital as well as analog regions of the devices.

Third, many different internal regions can latch, and it is necessary to observe very large numbers of latchup events with several different types of ions in order to get the proper picture of how latchup affects different regions of the part. Using power supply current detection and shutdown as a circumvention method is difficult for a device of this type because of the large number of different latchup paths that are present in the circuit along with the wide range of currents that occur for different latchup paths. It is necessary to monitor all power supplies and to consider variations in nominal operating current for different units and operating conditions in order to establish detection limits.

B. Catastrophic Failure Testing and Failure Modes

Relatively little attention has been given to determining the underlying reasons for catastrophic failure from latchup. One reason is that latchup is often used as a "go/no go" criterion for using parts in space. If ground tests show that a device is sensitive to latchup, often it is eliminated from further consideration. That is particularly true for devices that exhibit catastrophic failure.

Another factor relates to the way that latchup testing is done. Tests at high accelerators are costly, and nearly always require that the device is placed in a vacuum chamber at the exit port of the accelerator. If a device fails catastrophically, considerable time is required to open the chamber and pump it down after the device is changed. The goal of testing is usually to measure enough latchup events to determine the cross section. This cannot be done very easily if parts have to be continually changed because they are failing.

Latchup tests are usually done with special power control systems that sense the high-current condition just after it occurs, and shut down the power system shortly thereafter. Consequently the only catastrophic failure modes that will occur are those which involve currents that pass through the latched region for short time periods. Although it is possible to leave the device in a latched state, this is awkward and costly at accelerator facilities because of the high cost of beam time. When this is done, it is usually possible to investigate only a small number of conditions and current paths. Thus, attempts to determine catastrophic failure during tests at radiation facilities are usually of limited value.

Latchup causes a great deal of local heating within the sensitive region. However, unless the temperature is extremely high (> 500 ºC) it is unlikely that latchup will affect semiconductor, oxide or contact regions during time periods of a few minutes or hours, even though high temperature rises for short times may have an adverse effect on long-term reliability.

The weakest regions of most devices are the metallization and the bond wires. As discussed earlier, we found evidence of partial melting and recrystallization in many of the metallization regions of AD9260 devices after latchup tests were done, in addition to cases where the metallization path was clearly destroyed. None of the failures appear to be related to the semiconductor regions despite the large increase in local temperature that was observed during the thermal imaging experiments.

C. Metallization Failure

Laser tests of the AD9260 showed that failure only occurred for currents that exceeded 200 mA. Those failures tended to occur in specific regions of the device; failures in those same regions were observed in devices that had failed during tests with heavy ions. Even though there were numerous latchup sites with currents between about 40 and 200 mA, catastrophic failure was never observed in those regions, even when the device was latched repeatably with the pulsed laser. This implies that there is a threshold condition for metallization failure, somewhat above 200 mA for the AD9260. The metal lines where failure occurred were nominally 2 µm wide by 1 µm thick, as measured with a scanning electron microscope.

It is interesting to compare our results with a study of pulsed metallization failure that was done by Murguia and Bernstein in 1993 [17]. They investigated pulsed metallization failure conditions using special test structures. The metal lines in their study were 3 μm wide. They applied pulses for very short time periods (as short as 10 ns), They were able to determine the threshold conditions for failure by gradually increasing the current and/or time interval until failure was observed. Their tests showed that for electrical pulses between 10 ns and 1μs current density and time were inversely related. This corresponds to an adiabatic thermal condition, and effectively results in a total charge condition for catastrophic failure.

However, for pulses > 1 μs metallization failure was independent of pulse width, resulting in a threshold current density for failure -- essentially a critical current density -- that was approximately 10^7 A/cm^2. That is, once the pulse width exceeded 1 μs for a current density above the critical value the metallization region failed regardless of how long the electrical pulse was applied. Those results are shown in Figure 10. Our results for catastrophic latchup in the AD9260 are shown for comparison. Note that the current densities are nearly identical to those obtained from the test structures.

The Murguia and Bernstein result shows that unless one can detect and remove power from metallized regions in less than 1 μs, catastrophic failure will occur once the current density exceeds the critical value. That observation is consistent with our observations of failures from latchup where failure only occurred for currents above 200 mA. It also explains why no failures occurred in the AD9240: none of the latchup currents in the heavy ion tests of that device were high enough to exceed the critical current density threshold.

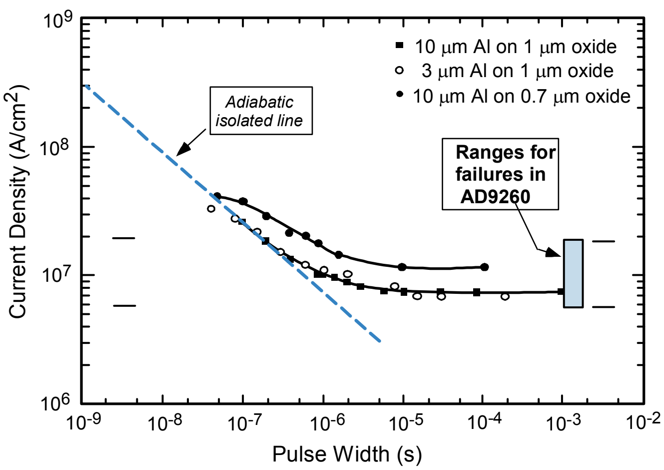


Figure 10. Critical current density for pulsed metallization failure (after Murguia and Bernstein [17]), along with the current densities where failure was observed during latchup tests of the AD9260.

Latent damage is another important issue. Our examinations of failed devices after laser tests showed many different regions where molten aluminum had been ejected from metallization, and catastrophic failure did not occur when functional tests were done afterwards. The size of the ejected metal spheres varied considerably, and many of them were much smaller in diameter than the width of the metallization lines. This raises the possibility that latchup testing -- or attempts to circumvent latchup by monitoring current and shutting down power -- may results in latent damage in the metallization. The results of our tests along with the metallization test structure results [17] suggest that there is no way to prevent this type of damage unless the power can be shut down in time intervals on the order of a few microseconds, which is difficult to do on circuit boards that contain large bypass capacitors on power supply lines.

V. Conclusions

This paper has discussed latchup in two types of analog-to-digital converters. Analog-to-digital converters are unlikely to be fabricated on epitaxial substrates because of noise considerations, and thus latchup is likely to remain a critical issue for that category of circuit.

Even though these two devices are fabricated with similar processes by the same manufacture, one of the device types exhibited catastrophic latchup. The failures were the result of localized melting of metallization, encased in silicon nitride, that ejected droplets of metallization laterally. There appears to be a critical current density for this type of failure. Failure occurred in one of the two types of converters because the equilibrium currents in some of the latchup paths exceeded the critical current density. Equilibrium currents in the other converter (as well as in many other latchup paths within the converter type that failed) were a factor of two or more below the critical current density, and appeared to be too low to cause catastrophic failure in any of the tests done in this study.

Although latchup mitigation techniques can sometimes be used for latchup-sensitive devices, considerable effort is required to ensure that these approaches are effective. The large number of latchup paths in modern circuits makes this approach particularly challenging. The observation of latent damage in metallization after latchup is another important concern when latchup-sensitive devices are used in space.

VI. Acknowledgment

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